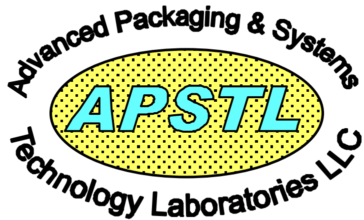
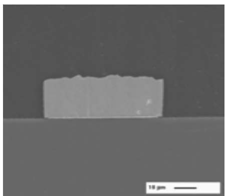
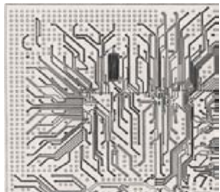


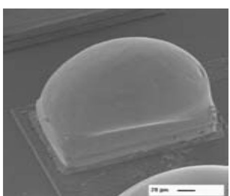
APSTL is your **reliable and affordable** resource for technologies essential to **Advanced Packaging**



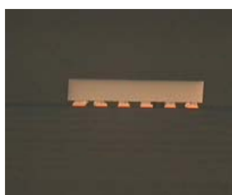
Electroplated solder bump technology



HD micro-via organic substrate w/ thermal vias



Solder capped Electroless Pedestal bumps



Flip chip die in Mobile Phones

Depend on ***APSTL*** *to implement* ***YOUR*** *Advanced Packaging Projects, from* ***Processors*** *to* ***Portables***

APSTL helps you to **implement** available Advanced Packaging technologies, as well as **Customize**, **Develop** and **License** new technologies and put them into **Production** at **Costs competitive** with outsourcing to **LCMR**

Low Cost Wafer Bumping Line engineered by ***APSTL*** in operation at the Wafer Fab of a US Customer

Robotic Flip Chip Assembly Line engineered by ***APSTL*** in operation at a US Customer site

APSTL **licensed** technology makes Advanced Packaging **economic** even at **low volumes** and **high labor cost**

APSTL can **CUSTOMIZE** available Advanced Packaging technologies to meet **YOUR** specific application, reliability and cost targets

APSTL technology enables **Product Differentiation** through **Customized** Packaging technology and ensures **protection of IP**

APSTL Services

- **For prospective Users of Advanced Packaging** :
  industry and technology roadmaps, competitor and supplier analyses, technology options, new package selection and development (in – depth evaluation of available technologies and infrastructure, modifications, thermal modeling) especially for SIP type applications, supplier management, incoming QC

- **For Suppliers of Packaging Materials, Tools etc.** :
  gap analyses to identify new business opportunities, integrated evaluation plans for their new products (materials, tools), technical and program management of evaluation / development

- **For Providers of Packaging Services** :
  demand analyses, gap analyses to identify new business opportunities (e,g. alignment with major drivers), turnkey science and engineering for various Wafer Bumping, High Density Substrates, New Package Configurations (SIP, 3-D), sound theoretical approach to design and integration (EMI, heat, stress, ..), Assembly / test, proven world class Program Management for start – up, Licensing of Technologies

- **Other Services**
  Training Courses on Advanced Packaging (also at select IEEE Conferences)

APSTL Technology Portfolio

- Wafer bumping utilizing a range of processes : electroplating, electroless, printing are in licensed production
- Early developer of electroplated solder bump FC technology (1989)
- Original developer (1994) of electroplated Column bumps down to 25 um sq. at 40 um pitch
- Column bumps for critical applications (large dies, weak dielectrics as in processors, memory) to overcome shrink issues (stress, underfill flow, electromigration)
- Electroless bump technology for cost driven consumer applications
- Wire bumps for prototyping
- Active Area bumps for heat extraction
- technology modifications to improve performance and yield of high density multi – layer organic substrates with micro – vias.
- Flip Chip Assembly : all aspects, including new process to create fatigue resistant joints
- mitigation of thermal and EM issues arising from integration in SIP Modules for mixed signal
- integrated passives and structures
- new package development

APSTL Core Competencies

- Technology and Industry trend analyses
- Technical economic analyses : cost – benefit trade - offs
- Package Selection & Qualification
- Rel Test and sophisticated Failure Analyses using various electron probes
- Materials science for solders, interconnect and dielectric materials,
- Application of Mathematics and Numerical Analyses to accelerate development (e,g. modeling and optimization of process, reliability, equipment design, ..)
- Statistical experimentation and quality control
- Design of factories and automation for wafer bumping, advanced substrates , flip chip assembly
- Selection, training and management of suppliers
- Training of Customer personnel, start – up and support
- Technical Marketing

APSTL offers YOU a solid track record in Advanced Packaging

- Developer (1989) at Motorola SPS (currently Freescale) of **world's first** Robotic Flip Chip Bonder (cost reduced by application of innovative algorithms) that was licensed and has now become the standard configuration
- Developer (1991 through 1997) of electroplated solder bump technology in use at Motorola and most other Microprocessors
- Developer (1994) of first high heat transfer flip chip technology for Gallium Arsenide Power Amplifiers that led to their use in Cell Phones
- Developed high density Organic substrates for Intel Microprocessors and Managed start up and ramp (1998) at overseas Suppliers
- Developed at APSTL (2001 -) low cost reliable electroless Ni – P wafer bumping for mobile phone applications, in production at small semiconductor companies,
- Turnkey engineering and start up of Fabs (2002 -) for above
- Flip chip assembly line (2004)
- Chairing IEEE ECTC session on Pb – free Flip Chip
- Developed at APSTL high reliability version of electroless Ni – P bumps for WLP

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